9210-117
Level 6 Graduate Diploma in Engineering
Electronic systems

Sample Paper

You should have the following for this examination
- one answer book
- non-programmable calculator
- pen, pencil, drawing instruments

No additional data is attached

General instructions
- This examination is of **three hours** duration.
- The paper contains **nine** questions.
- Answer any **five** questions.
- All questions carry **equal** marks. The maximum marks allocated to each part within a question are shown alongside.
- Electronic calculators of the non-programmable type may be used. However, the candidate is expected to indicate sufficient calculation steps on paper to justify the answer.
- Candidates are encouraged to use diagrams wherever appropriate to supplement their answer even if a question does not particularly instruct to do so. All drawings should be neat, in good proportion and properly labelled where applicable.

1 a) The voltage – current relationship for a silicon diode is mathematically modelled as follows,

$I = I_0(e^{\frac{kV}{zT}} - 1)$ where $k = 11{,}600\ \text{KV}^{-1}$

V is the voltage across the diode.
I is the diode current.
T is the absolute temperature.

i) Show that when the diode is forward biased with a voltage comparatively larger than 2T/k,

$I = I_0\, e^{\frac{kV}{zT}}$ (2 marks)

ii) Show that when the reverse bias voltage increases,

$I \rightarrow -I_0$ (2 marks)

b) Usually when I – V characteristics of a semiconductor diode are plotted, different scales are used for the positive and negative directions of the current axis.

i) Explain why this is done. (3 marks)

ii) Sketch the I – V characteristics for a silicon diode indicating the important parameters. (3 marks)

c) Figure Q1.1 shows an arrangement where 5 silicon diodes are used to obtain a voltage reference of 3 V.

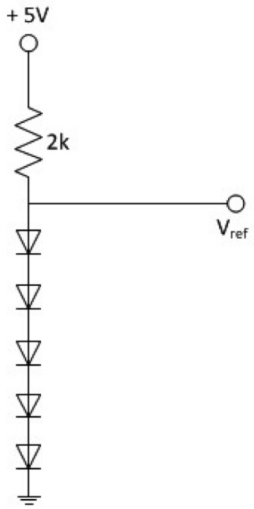

Figure Q1.1

i) Estimate the cut-in voltage for a silicon diode. (5 marks)

ii) If the forward resistance of a silicon diode is 20 Ω, calculate the total power dissipation across the diodes. (5 marks)

2 a) i) Draw the magnified view of the area **close to the origin** of the characteristic curves for a junction FET so that the variation of drain current with very small values of the drain to source voltage for different values of gate to source voltage is visible. (3 marks)

ii) Hence, show that a J-FET can be used as a **voltage controlled resistor** for very low values of drain to source voltage. (2 marks)

b) The a.c small signal drain current of a J-FET i_d can be expressed as a function of the small signal gate to source voltage v_{gs} and the drain to source voltage v_{ds}, as follows,

$$i_d = g_m v_{gs} + \frac{1}{r_d} v_{ds}$$

where g_m is the trans conductance and r_d is the a.c. drain resistance of the J-FET.

Describe how g_m and r_d could be estimated from the characteristic curves of the J-FET. (5 marks)

c) Figure Q2.1 shows the front-end circuit of a high impedance-measuring instrument that employs a junction FET.

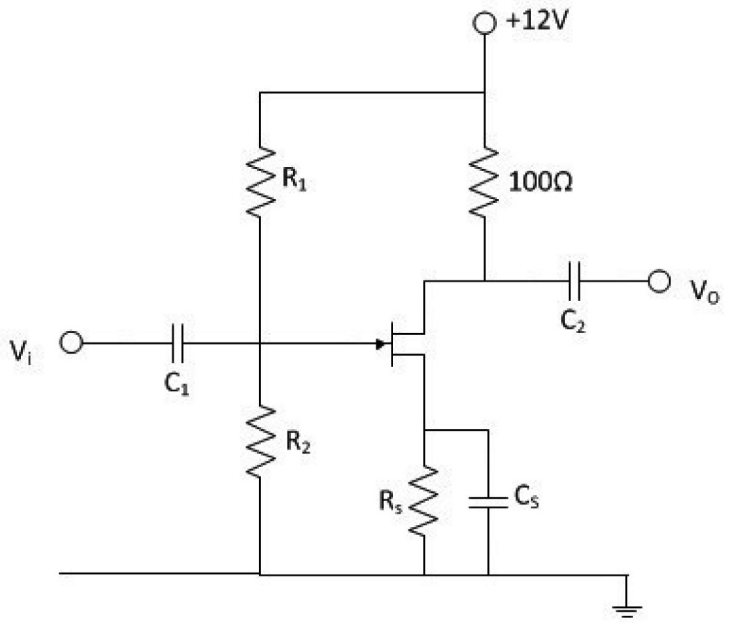

Figure Q2.1

i) Briefly explain why a J-FET has been chosen as the active element in this circuit. (2 marks)

ii) Draw the small signal a.c. equivalent circuit for this front end. (3 marks)

iii) If g_m = 0.5 mS and r_d = 100 kΩ for the J-FET, calculate the voltage gain of this front end. (5 marks)

See next page

3 a) i) A bipolar transistor is used as a Common Emitter amplifier. Using the transistor dc characteristics, explain what is meant by the '**operating point**' of the transistor. (3 marks)

ii) When common emitter bipolar transistor amplifiers are used in low power applications the transistor is biased such that the operating point is located towards the middle of the characteristics plane. Explain why this is done. (3 marks)

b) Figure Q3.1 shows an npn transistor working as a C-E amplifier with a simple bias arrangement that uses a single resister R. The d.c. current gain β of this transistor is 40.

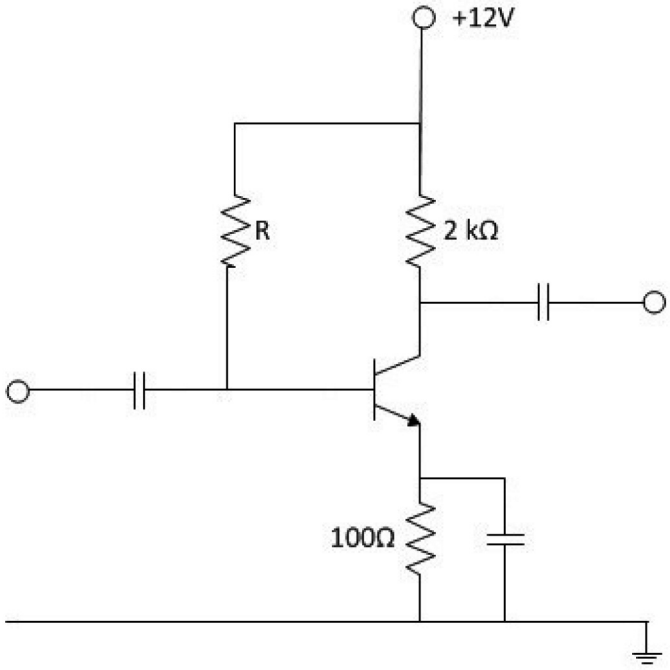

Figure Q3.1

i) If it is required to fix the operating point so that V_{CE} is equal to half the supply voltage, write the equations required to determine the corresponding base current. (4 marks)

ii) Hence, determine the value of the resistor R that would provide the required base current. (2 marks)

c) i) For the transistor in the amplifier given in Figure Q3.1, if h_{ie} = 1.2 kΩ and if h_{re} and h_{oe} are negligible, draw the small signal a.c. equivalent circuit for this amplifier. (3 marks)

ii) Hence, calculate the voltage gain of this amplifier when no load is connected at the output. (3 marks)

iii) State the assumptions made in your answer to part ii) above. (2 marks)

4 a) State why constant current sources are often used in place of bias resistors in bipolar transistor integrated circuits. (2 marks)

b) Figure Q4.1 shows a constant current source constructed using a silicon npn transistor and two silicon diodes.

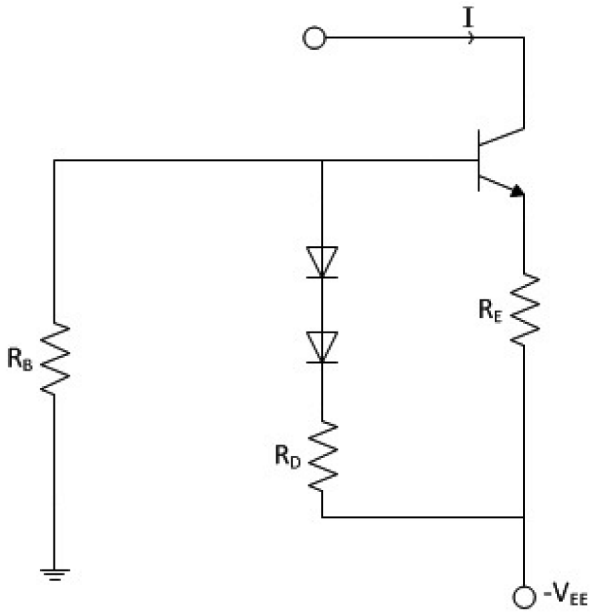

Figure Q4.1

i) If the cut-in voltage of each diode is V_D and the base - emitter voltage of the transistor is V_{BE}, neglecting the base current, write equations to determine the current through the diodes. (6 marks)

ii) Hence obtain an expression for the collector current *I*. (4 marks)

iii) Deduce the relationship between V_D and V_{BE} in order to make *I* constant. (4 marks)

c) Briefly explain why two diodes are used in the above circuit. (4 marks)

See next page

5 a) i) Explain what is meant by the '**Dynamic Range**' of a two port electronic device. (3 marks)

ii) The pre-amplifier of an airborne navigational aid receiver has to operate satisfactorily when it is very far away from the transmitter as well as when it is very close to the transmitter. Show that this pre-amplifier requires to have a large dynamic range. (3 marks)

b) i) Draw the circuit for an **inverting** amplifier that uses an ideal op-amp. (2 marks)

ii) Draw the ideal equivalent circuit for this amplifier. (2 marks)

iii) Hence, obtain an expression for the voltage gain. (2 marks)

c) Figure Q5.1 shows a passive electronic component whose I-V characteristics are defined by the equation,

$I_x = I_0 e^{\frac{V_x}{V_T}}$, Where V_T and V_0 are constants.

Figure Q5, 2 shows this component used with an ideal op-amp to construct a special type of amplifier to support a large dynamic range for the input.

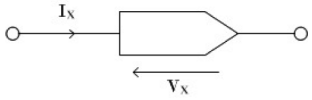

Figure Q5.1

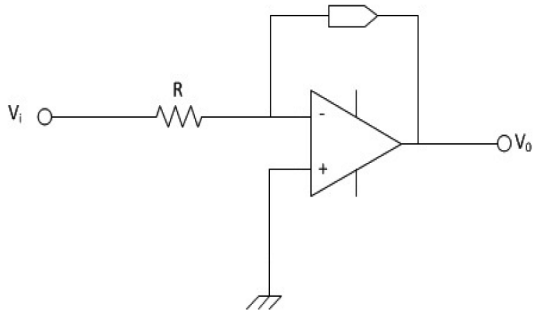

Figure Q5.2

i) Obtain an expression for the output voltage v_0 of this amplifier. (4 marks)

ii) Hence, show that the output voltage is proportional to the logarithm of the input voltage. (2 marks)

iii) Using example values describe how this amplifier compresses a large range of input voltages into a small range of output voltages. (2 marks)

6 a) i) List the values of the input impedance, output impedance and open loop differential gain of an ideal op-amp. (3 marks)

ii) Hence, using the equivalent circuit, show that a virtual short circuit exists between the two inputs of an ideal op-amp when in operation. (3 marks)

b) Figure Q6.1 shows a waveform generator that uses two ideal op-amps.

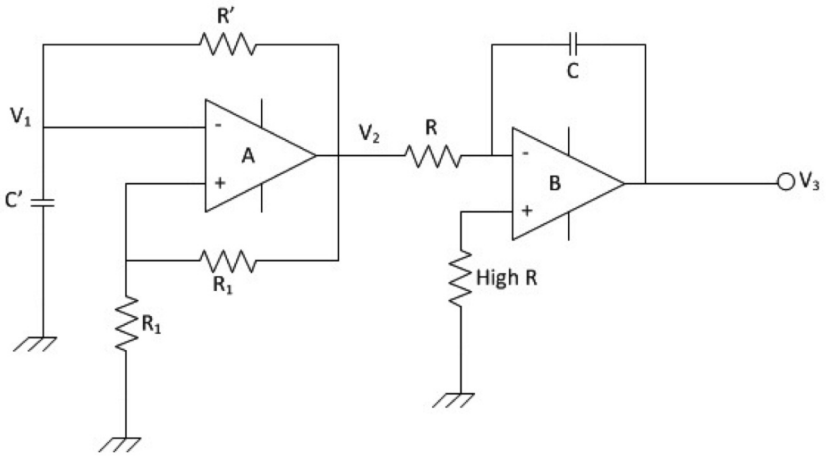

Figure Q6.1

i) Using the equivalent circuit for an ideal op-amp, obtain an expression for the output voltage v_3 in terms of the inter-stage voltage v_2. (3 marks)

ii) Hence, show that op-amp 'B' functions as an integrator. (3 marks)

iii) Draw the waveforms of the voltage v_1, v_2 and v_3 on a common time base to illustrate the operation of this circuit. (6 marks)

c) Identify the op-amp that operates in the 'linear mode'. (2 marks)

7 a) Explain one advantage of using Read Only Memories (ROM) instead of logic gates to implement combinational logic circuits. (2 marks)

b) A gaming machine requires the following signals derived from 4 logic inputs X_0, X_1, X_2 and X_3.

- A Majority vote - detector output 'Y' that becomes '1' whenever the majority (more than 2) of the 4 inputs are '1'.
- A tie – detector output 'Z' that becomes '1' whenever the 4-bit input combination has an equal number of '1s' and '0s'.

i) Write the truth table for the two outputs 'Y' and 'Z'. (4 marks)

ii) Using Karnaugh maps or otherwise, deduce the simplified Boolean expressions for the two outputs 'Y' and 'Z'. (4 marks)

iii) Implement the circuit for output 'Y' using only NAND gates. (4 marks)

c) An alternative implementation of the above two circuits is to be done using a ROM with the two least significant bits of the data bus of the ROM representing the binary number YZ and the four least significant bits of the address bus of the ROM representing the binary number $X_3X_2X_1X_0$.

i) Write one possible programming chart for the first 16 locations of the ROM using hexadecimal notation. (4 marks)

ii) Describe the precaution that could be used to prevent the remaining locations of the ROM being accidentally addressed. (2 marks)

See next page

8 a) A web article on digital systems contained the statement '**Sequential circuits possess memory**'
Briefly explain what this statement means. (2 marks)

b) Figure Q8.1 represents the incomplete state diagram of a sequential circuit used to check whether the first bit of non-overlapping 2-bit sequences in an incoming bit stream is '1'. The indication should be made on reception of the second bit.

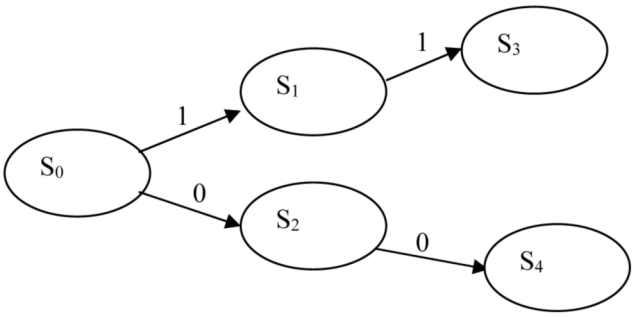

Figure Q8.1

i) Copy the figure to your answer script and complete the state diagram by zdrawing the remaining transitions. (4 marks)
ii) Write the state table for the completed state diagram. (4 marks)
iii) Deduce the optimum state table by applying state reduction. (2 marks)

c) Figure Q8.2 shows the state diagram for a 3-bit grey code generator that uses 3 Delay flip-flops. The number shown within each state is the binary number $Q_2Q_1Q_0$ represented by the flip-flop outputs.

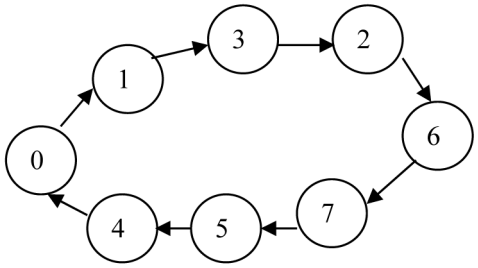

Figure Q8.2

i) Indicate the state transitions for the 3 flip flops on a single table, clearly showing the flip-flop outputs before and after the n^{th} clock pulse. (4 marks)
ii) Hence, design combinational circuits for the inputs of all 3 flip-flops. (4 marks)

9 Figure Q9.1 shows the simplified circuit of a single channel data acquisition system. The input is an analogue voltage and the programmer is a 4-bit **successive approximation** binary sequence generator.

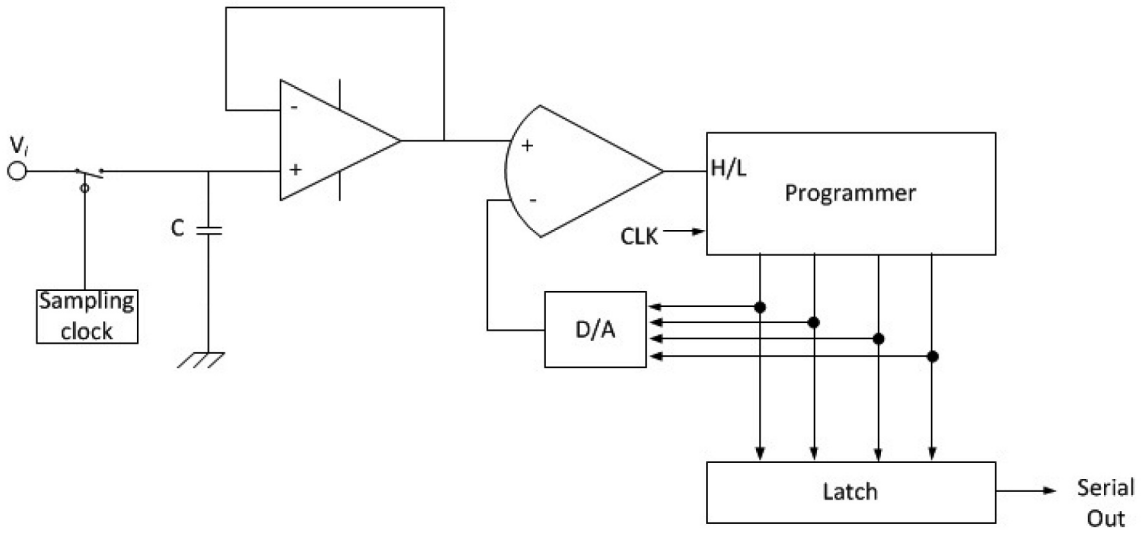

Figure Q9.1

a) Briefly explain the need to have the op-amp between the capacitor and the comparator input. (2 marks)

b) The generator produces full scale reading for an analog input of 30 mV. Write down the binary sequence generated when the following analogue inputs are applied.

i) 21.5 mV (3 marks)

ii) 5.4 mV (3 marks)

c) i) What would be the output of the D/A when the programmer produces the reading 0110_2? (2 marks)

ii) Draw the waveform of the H/L input to the programmer when the analogue input is 2.5 mV. (5 marks)

iii) If the minimum time gap between two analogue samples is 2 ms and if the programmer should produce a stable reading at least at the middle of this time gap, calculate the minimum clock frequency of the programmer. (5 marks)