City & Guilds

9210-123
Level 6 Graduate Diploma in Engineering
Computer architecture and operating system

Sample Paper

You should have the following for this examination • one answer book • non-programmable calculator • pen, pencil, ruler, drawing instruments	**No additional data is attached**

General instructions
- This examination paper is of **three hours** duration.
- This examination paper contains **nine** questions.
- Answer **any five** questions.
- All questions carry equal marks. The maximum marks for each section within a question are given against that section.
- An electronic, non-programmable calculator may be used, but the candidate **must** show clearly the steps prior to obtaining final numerical values.
- Drawings should be clear, in good proportion and in pencil. Do **not** use red ink.

1 a) There are different C compilers available for various vendor specific processors, provide the reasons for having different C compilers. (5 marks)

b) Calculate the minimum memory required to hold the data of the following program when executing. Sizes of the data types are given below.

```
#include <stdio.h>
void main ()
{
char message[] = “Come Home”;
rintf(”%s”,message);
}
```

char – 8 bits
int – 16 bits (5 marks)

c) Write a C program to add ASCII values of “H” and “C”. (5 marks)

d) Consider the ASCII values given in the following table and write the outputs of the following C program.

ASCII	**Char**	**ASCII**	**Char**
64	@	73	I
65	A	74	J
66	B	75	K
67	C	76	L
68	D	77	M
69	E	78	N
70	F	79	O
71	G	80	P
72	H	81	Q

```
#include <stdio.h>
int main ()
{
int d = 70;
for(int i=0;i<5; i++){
int r = d + i;
printf(”%c”,r);
}
return 0;
}
```

(5 marks)

2 a) Write the following steps in an instruction execution cycle according to their correct order.

Execute
Calculate the address of the operands (if any)
Store result in memory
Calculate address of the result
Extract the operand from memory (5 marks)

b) Draw a basic organization of a computer system by using Control Unit, Arithmetic and logic Unit, Memory, Inputs and Outputs. Indicate the control signals and data signals separately. (5 marks)

c) Write **five** main functions of a control unit. (5 marks)

d) What are the main features of a **hardwired** control unit? (5 marks)

3 a) Compare and contrast Von-neumann architecture with Harvard architecture? (5 marks)
b) Briefly describe the use of accumulator register inside an ALU. (5 marks)
c) A particular ALU uses 8 bits registers for all the operations and to store results. In an instruction execution, a multiplication operation of 40 x 100 was performed. Describe the status change of Flag register. (5 marks)
d) Represent –5.125 in IEEE 754 single precision format. (5 marks)

4 a) Non-pipelined processor can be transferred to processor with a large number of pipelined stages, but it has some disadvantages. State the disadvantage according to the above situation. (5 marks)
b) Non-pipelined processor with 40 ns of instruction cycle time was divided into 5 pipelined stages with 2 ns of latch latency in each stage. Calculate the time taken for an average instruction to complete its operation. (5 marks)
c) What is the latency in between two consecutive instructions in above pipelined processor in part b). (5 marks)
d) What is the maximum speedup possible from the pipelined processor in part b)? (5 marks)

5 a) A computer program contains 75% of division operations which runs within 120 s. and it is possible to improve the speed of division operations. There is a need to make the program 1.5 times faster. How much speedup of division instructions should be achieved to allow the expected speedup? (5 marks)
b) What is the new program run time after the improvement? (5 marks)
c) Calculate the maximum overall speedup possible by the above setup in part a). (5 marks)
d) Assume that the speed up of division instructions was improved by 2 times, calculate the overall speedup of the program. (5 marks)

6 a) Compare and contrast Direct memory access with random memory access. (5 marks)
b) What are the main features of Big endian memory storage. (5 marks)
c) A hypothetical computer memory system contains a 32 bit memory word 0x122db1b1 in addresses from 8000 to 8003. The system uses byte addressible memory organisation in big-endian byte order. Assign the relevant data bytes to corresponding memory addresses. (5 marks)
d) Categorise the following memory devices into onboard, out-board and external categories.
USB Drive, Hard disk, level 2 caches, DDR-II DRAM, Storage Area Network (SAN), DVD. (5 marks)

7 a) Compare and contrast Direct addressing and Register addressing. (5 marks)
b) Why is the RISC instruction execution faster than CISC? (5 marks)
c) A memory system contains two levels (level 1 and level 2) of memory where the access times are T1 and T2 respectively. Level 1 memory is closer to the processor and maintains hit ratio of H. Accessing level 2 memory needs to go through level 1. Derive an equation to evaluate average access time (TA) of this memory system. (5 marks)
d) According to the system given in part c), if level 2 memory access time T2 is two times of T1, obtain an expression for memory access efficiency. (5 marks)

See next page

8 a) Briefly describe the UNIX operational command given below.

```
ls -l > abc.txt
```

(5 marks)

b) What is the use of the following command in Windows?

```
attrib +r my.bat
```

(5 marks)

c) What is the purpose of using sudo command in Unix systems? (5 marks)

d) In Stack based instruction execution system, evaluate the result of the following program. (5 marks)

```
PUSH #8
PUSH #2
PUSH #14
DIV
PUSH #10
ADD
SUB
```

9 a) Briefly Describe the **three** state process model in an Operating System. (5 marks)

b) How is multi-tasking achieved on a uniprocessor system? (5 marks)

c) What is a race condition? Give an example. (5 marks)

d) What is an interrupt in an operating system environment? (5 marks)