City & Guilds

9210-213
Level 7 Post Graduate Diploma in Engineering
Digital system design

Sample Paper

You should have the following for this examination
• one answer book

No additional data is attached

General instructions
• This paper consists of **eight** questions.
• Answer **five** questions.

1 a) Hardware Description Language (HDL) allows the representation of a digital system at different levels of abstraction such as at circuit level (referred to as structural representation), data flow level and at behavioral level (referred to as behavioral representation).
Taking 1 bit Full Adder as an example, do the following:

i) Draw the circuit diagram using 2 and 3 input logic gates as appropriate. (3 marks)

ii) Use Verilog HDL code to implement the 1-bit Full Adder using Structural, Dataflow and Behavioral representation. (9 marks)

b) i) Outline three advantages of single chip prototyping based on HDL over the traditional approach of discrete component based logic design. (3 marks)

ii) HDLs are generally meant for two purposes, namely, simulation of digital systems and for synthesis. The language features of HDL, often, are on par with most of the high level languages. However there can be instances where HDL code which can be properly simulated might not be synthesizable. Critically analyze the above statement considering high level language features and illustrating with appropriate code examples. (5 marks)

2 a) i) Carry Look-Ahead Adder (CLA) makes use of a Carry Look Ahead unit to compute the carry necessary for addition making it much faster than a ripple adder. Write a Verilog module for a 4-bit CLA. (6 marks)

ii) Using the 4 bit CLA in 2 a) i) above, write a Verilog module to represent an 8-bit CLA using two cascaded 4-bit CLAs. (4 marks)

b) i) Use of HDL is a way for rapid prototyping of digital systems. In this context, testbenches play a significant role in determining the success of the process. Critically analyze the role of testbenches in the design process. (3 marks)

ii) Write the Verilog code for a sequence detector for the code 1001 (with overlapping) that would result in the minimal hardware and a testbench to test the design. (7 marks)

3 Two waveforms are given as inputs to a Digital System. One is a clock signal **Ck** and the other is a digital signal **(A)** which is synchronized with the falling edge of the clock signal (ie rising and falling edge A is synchronized to the falling edge of the clock signal).
A sequence detector is to be designed to detect two consecutive zeros or two consecutive ones (ie clock signal will sample input digital signal at each rising edge and the value at that point is considered for the detection). In each case, output should be high. The system should return to the initial state when detection of the sequence is done.

a) Draw the clock, digital input and output waveforms to illustrate the operations of the system. (6 marks)

b) Draw a Finite State Machine to represent the above system. (8 marks)

c) Write Verilog HDL representation of the above system. (6 marks)

4 Automotive adaptive cruise controllers have become popular due to the convenience it provides to drivers on highways that has average traffic. It allows the vehicle to automatically adjust the speed of the vehicle depending on the distance to the front vehicle. A key module of this controller is a laser based distance measurement unit. You are required to design this module that can measure distance up to 2 km.
The module has the following features:

- The system has two inputs – 1-bit input **B** that starts measurements when the user put the vehicle into adaptive cruise controller mode. The second 1-bit input S comes from the sensor that detects the reflected laser.
- The Output (1-bit) **L** controls the laser turning it on when L is 1. Finally N-bit output **D** gives the distance measurement to the main controller module.

The laser will be on for 1 clock pulse when it is turned on. The unit will start counting clock cycles until the sensor detects the reflected pulse.

a) Design a high level state machine for the distance measurement unit. (8 marks)
b) Suggest a value for **N** (counter). Explain the basis for your answer. (4 marks)
c) Draw a clearly labelled datapath with all the required components, necessary control signals and connections to the control unit. (Note: You are not required to carry out detailed controller design). (8 marks)

5 a) Instruction Set Architecture (ISA) refers to the design of Instruction Set of a processor.
   i) Describe the key elements of an instruction. (2 marks)
   ii) Using 3 examples, explain the meaning of addressing mode and its importance in the execution of an instruction. (7 marks)
b) i) Explain Load and Store Architecture using appropriate examples. (3 marks)
   ii) Explain Stack-based Architecture using appropriate examples. (3 marks)
   iii) Explain the meaning of Register Windowing. (5 marks)

6 Consider the following arithmetic expression:
$Y = ((A + B) * C)/(D – (E * F))$
(The operators +, -,* and / have their usual meaning)
The integer variables A,B,C,D,E and F are stored in consecutive memory locations starting from memory address 1000 and each takes 4 bytes. The output Y is stored at the memory address 1100. Assume the availability of a number of general purpose registers and the following commands : LOAD, STORE, MOV, POP, PUSH (Data transfer) ADD, SUB, DIV and MUL (Arithmetic Instructions) with the commands having their usual meanings.

a) Assuming a Load and Store Architecture, list the sequence of assembly level instructions that would implement the above expression using 3 address instructions. (7 marks)
b) List the sequence of assembly level instructions assuming a Stack Based Architecture. (7 marks)
c) Referring to the number of memory references in a) and b), explain which architecture is preferred for an application that requires a high throughput. (6 marks)

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7 a) i) Explain the meaning of Semantic Gap and its significance in processor design. (3 marks)

ii) Using an appropriate instruction as an example, explain Mirco-programming approach to processor design. (4 marks)

iii) Describe the key elements of a Processor data path. (3 marks)

b) A custom processor has the following requirements:

- Two port Memory Access for Program and Data Memory with 2 dedicated pairs of registers for address and data/instruction.
- Load and Store Architecture with 3 address ALU instructions
- ALU with a support for 16 different operations.
- 8 General Purpose 32 bit Registers.
- Stack Pointer to access Data Stack.

i) Draw a clearly labelled processor datapath. (7 marks)

ii) Compute the number of control signals required to operate this datapath. (3 marks)

8 An embedded processor, to be used in an environment where responsiveness is a major concern, plans to make use of cache to improve the memory access time. It has the following specifications:

- 16 bit data and address bus.
- Maximum amount of DRAM that can be accessible through the given address bus.
- 8KB Cache.
- 16 byte block size (cache line size).

a) Assuming cache is organized with 2-way set-associative mapping, clearly list the steps it takes to read and write to the following memory locations in consecutive memory accesses. Assume the cache is empty at the beginning.
You need to clearly indicate whether the access results in a cache miss or cache hit and cache tag values for each access.

i) 0xABC0 (READ).

ii) 0xABC2 (WRITE).

iii) OxABCE (READ). (12 marks)

b) Cache replacement algorithm is a key component of the entire cache design. Least Recently Used is one such algorithm. Briefly describe a possible implementation of this algorithm in hardware. (5 marks)

c) Briefly comment on the effect of block size and number of blocks in a set on cache performance. (3 marks)